

Please amend the claims as indicated below:

1-3. (Cancelled)

4. (Currently Amended) A system for verifying a plurality of systems on a plurality of chips, said system comprising:

a hardware emulator for verifying a first system on a chip and a second system on another chip, said hardware emulator comprising:

a first circuitry configured to realize and verify the first system on a chip, said first circuitry further comprising at least one output port for providing verification results from the first circuitry; and

a second circuitry configured to realize and verify the second system on another chip while the first circuit verifies the first system on chip, the second circuitry directly connected to the first circuitry.

5. (Original) The system of claim 4, wherein the hardware emulator further comprises:

a first interface operably connected to the first circuitry, wherein the first interface provides inputs to the first circuitry and receives outputs from the first circuitry; and

a second interface operably connected to the second circuitry, wherein the second interface provides inputs to the second circuitry and receives outputs from the second circuitry.

6-11. (Cancelled).

12. (New) The system of claim 4, wherein verifying the plurality of systems further comprises detecting errors in the plurality of systems.